

February 1992 Revised June 2001

74LVQ373

Low Voltage Octal Transparent Latch with 3-STATE Outputs

General Description

The LVQ373 consists of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable $(\overline{\text{OE}})$ is LOW. When $\overline{\text{OE}}$ is HIGH, the bus output is in the high impedance state.

Features

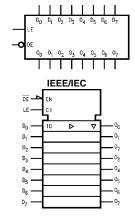
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- \blacksquare Guaranteed incident wave switching into 75 $\!\Omega$
- 4 kV minimum ESD immunity

Ordering Code:

Order Number Package Number			Package Description
	74LVQ373SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
	74LVQ373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
	74LVQ373QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Pin Descriptions

	Pin Names	Description				
D ₀ –D ₇		Data Inputs				
	LE	Latch Enable Input				
	ŌĒ	Output Enable Input				
	O ₀ -O ₇	3-STATE Latch Outputs				

Connection Diagram



Truth Table

	Inputs	Outputs	
LE	OE	D _n	O _n
Х	Н	Х	Z
Н	L	L	L
Н	L	Н	Н
L	L	X	O ₀

H = HIGH Voltage Level L = LOW Voltage Level

Z = High Impedance X = Immaterial

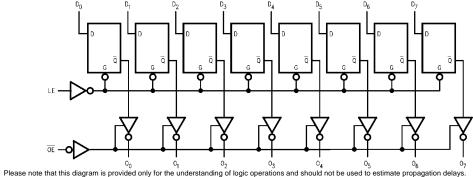
O₀ = Previous O₀ before HIGH to Low transition of Latch Enable

Functional Description

The LVQ373 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_{n} inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW, the latches store the information that was present on the D-type inputs a setup time preceding the

HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage (V $_{CC}$) -0.5V to +7.0V

DC Input Diode Current (I_{IK})

 $\begin{array}{ccc} V_{I} = -0.5V & -20 \text{ mA} \\ V_{I} = V_{CC} + 0.5V & +20 \text{ mA} \\ \text{DC Input Voltage (V_{I})} & -0.5V \text{ to V}_{CC} + 0.5V \end{array}$

DC Output Diode Current (I_{OK})

 $V_{O} = -0.5V$ -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) -0.5V to $V_{CC} + 0.5V$

DC Output Source

or Sink Current (I_O) $\pm 50 \text{ mA}$

DC V_{CC} or Ground Current

 $(I_{CC} \text{ or } I_{GND})$ $\pm 400 \text{ mA}$

Storage Temperature (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$

DC Latch-Up Source or

Sink Current ±300 mA

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC}) 2.0V to 3.6V Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_D)

Output Voltage (V_O)

Operating Temperature (T_A) -40° C to +85°C

Minimum Input Edge Rate (ΔV/Δt)

 V_{IN} from 0.8V to 2.0V

 $V_{CC} @ 3.0V$ 125 mV/ns

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Symbol	raiametei	(V)			ranteed Limits	Oilles		
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
	Output Voltage	3.0		2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH} \text{ (Note 3)}$ $I_{OH} = -12 \text{ mA}$	
V _{OL}	Maximum Low Level	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
	Output Voltage	3.0		0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH} \text{ (Note 3)}$ $I_{OL} = 12 \text{ mA}$	
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μА	$V_I = V_{CC},$ GND	
I _{OLD}	Minimum Dynamic	3.6			36	mA	V _{OLD} = 0.8V Max (Note 5)	
I _{OHD}	Output Current (Note 4)	3.6			-25	mA	V _{OHD} = 2.0V Min (Note 5)	
Icc	Maximum Quiescent Supply Current	3.6		4.0	40.0	μΑ	$V_{IN} = V_{CC}$ or GND	
I _{OZ}	Maximum 3-STATE Leakage Current	3.6		±0.25	±2.5	μА	$\begin{aligned} & V_{I}\left(OE\right) = V_{IL}, \ V_{IH} \\ & V_{I} = V_{CC}, \ GND \\ & V_{O} = V_{CC}, \ GND \end{aligned}$	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8		V	(Note 6)(Note 7)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.3	-0.8		V	(Note 6)(Note 7)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Note 6)(Note 8)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Note 6)(Note 8)	

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}) , 0V to threshold (V_{IHD}) , f = 1 MHz.

AC Electrical Characteristics

	Parameter		$T_A = +25$ °C $C_L = 50 \text{ pF}$			$T_A = -40$ °C to +85°C $C_L = 50$ pF		Units
Symbol		v _{cc}						
		(V)	Min	Тур	Max	Min	Max	
t _{PHL}	Propagation Delay	2.7	2.5	9.6	14.8	2.5	16.0	ns
t _{PLH}	D _n to O _n	3.3 ± 0.3	2.5	8.0	10.5	2.5	11.0	115
t _{PLH}	Propagation Delay	2.7	2.5	9.6	16.9	2.5	18.0	ns
t _{PHL}	LE to O _n	3.3 ± 0.3	2.5	8.0	12.0	2.5	12.5	110
t _{PZL}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	20
t _{PZH}		3.3 ± 0.3	2.5	8.5	13.0	2.5	13.5	ns
t _{PHZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
t _{PLZ}		3.3 ± 0.3	1.0	9.0	14.5	1.0	15.0	115
toshl	Output to Output Skew	2.7		1.0	1.5		1.5	ns
t _{OSLH}	(Note 9)	3.3 ± 0.3		1.0	1.5		1.5	115

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

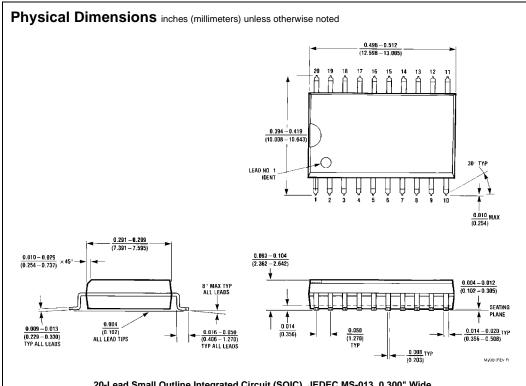
AC Operating Requirements

Symbol	Parameter	v _{cc}	$T_A = +25$ °C $C_L = 50 \text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$	Units	
		(V)	Тур	Guaran	teed Minimum		
t _S	Setup Time,	2.7	0	4.0	4.5	ns	
	HIGH or LOW	3.3 ± 0.3	0	3.0	3.0	115	
t _H	Hold Time,	2.7	0	1.5	1.5	20	
	HIGH or LOW	3.3 ± 0.3	0	1.5	1.5	ns	
t _W	LE Pulse Width,	2.7	2.4	5.0	6.0		
İ	HIGH	3.3 ± 0.3	2.0	4.0	4.0	ns	

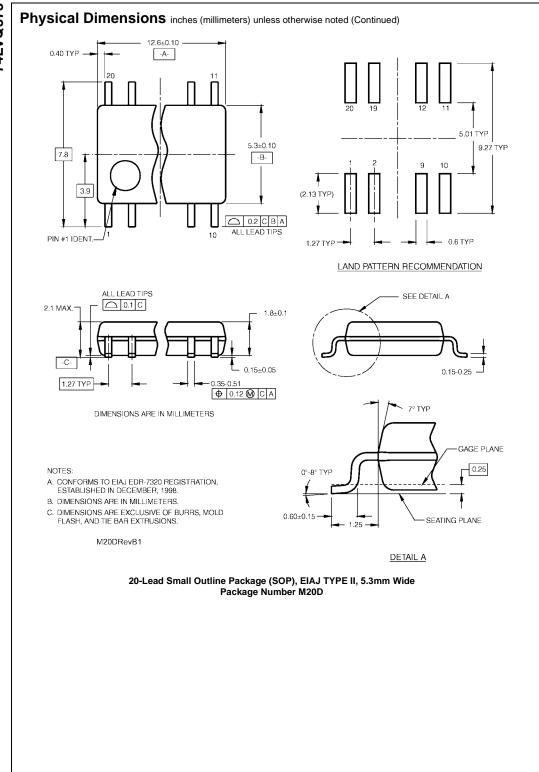
Capacitance

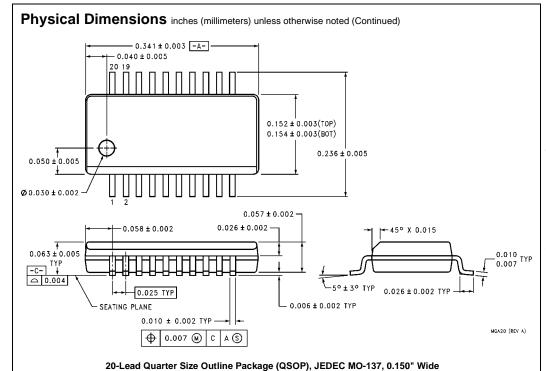
Symbol Parameter		Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	39	pF	V _{CC} = 3.3V

Note 10: C_{PD} is measured at 10 MHz.



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B





Package Number MQA20

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